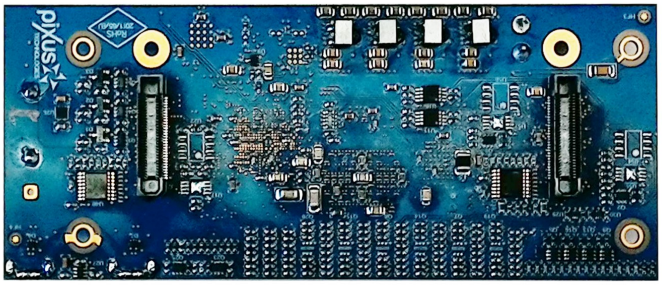
OpenVPX / SOSA Aligned Chassis Manager—Mezzanine

SHM300 Chassis Management Card



SHM300 KEY FEATURES

- Designed for OpenVPX systems and aligned to the SOSA™ Technical Standard
- Tier 3+ version
- Compliant to VITA 46.11 for VPX System Management
- SlotSaver design to fit as mezzanine behind backplane without taking up a slot
- Allows full access of VITA 66/67 P2 interfaces (RF and Optical housings) on backplane
- Chassis Discovery of Chassis FRU Information Storage Options (physical/backplane)
- Redundant, bussed System IPMB
- Cooling Management using VITA 46.11 fan control messages
- FRU discovery/confirmation and SDR-based sensor initialization
- Full Sensor Data Repository (local cache)
- Chassis Control & Event handling
- PolarFire® FPGA
- Icicle Kit development version available for prototyping in test/dev enclosure
- Customized versions available

Pixus offers OpenVPX Chassis Managers in standard designs as well as customized form factors. The SHM300 is a highly configurable Chassis Management Controller (ChMC) that targets VITA 46.11, Hardware Open Systems Technologies (HOST), C5ISR/EW Modular Open Suite of Standards (CMOSS), and Sensor Open System Architecture (SOSA) system management capabilities in an OpenVPX environment. The versatile approach allows the implementation of Tier 3+ requirements.

Similar to VITA 46.11, the SOSA aligned chassis manager interfaces across the IPMB bus on the backplane to monitor plug in cards (that have an IPMC), re-boot modules, control fan speeds, etc.

Optional features include chassis manager centric authentication and attestation, anti-tamper features, a JTAG multiplexing interface, and other secure out-of-band features.

Conformal coating on the SHM300 OpenVPX Chassis Manager is optional.

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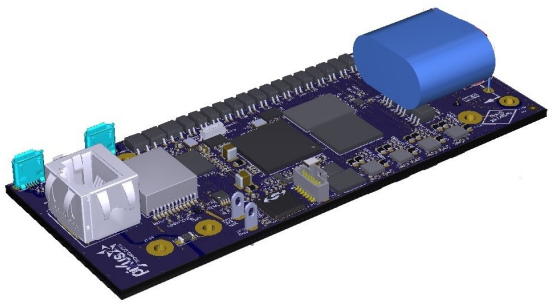
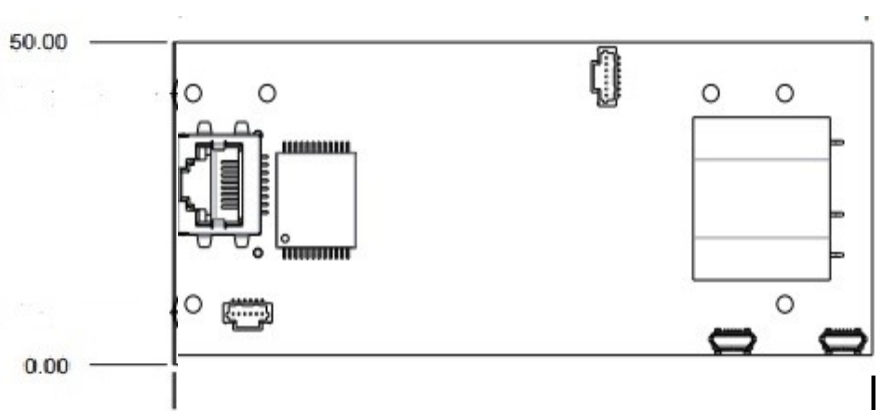
Specifications

Architecture		
Physical	Dimensions	~121.6 mm x 50mm, per VITA 48 for 3U pluggable version
		Other form factors available (consult factory)
	Panel Interface	LEDs, RJ-45, & USB interface
Standards		
VITA	Type	VITA 46.11, SOSA Technical Standard
		Pluggable version per VITA 48.1, VITA 48.2
Configuration		
Power Usage		1.3W at idle, under 5W typical (preliminary data)
Environmental	Temperature	Operating temperature: 0 to 70C, (extended temperature option of -40° to +85C—consult factory)
		Storage temperature: -55° to +100°C
	PCB	FR-4 or equivalent
Conformal coating		Upon request (See page 6 selection "J" for available options)
Other		
MTBF	MIL Handbook 217-F @ TBD Hrs.	
Certifications	Designed to meet CE and EN/UL/TUV certifications where applicable	
Warranty	Two years	
Trademarks and logos	The Pixus Logo is a registered trademark of Pixus Technologies Inc. other registered trademarks are the property of their respective owners. Specs. subject to change without notice.	

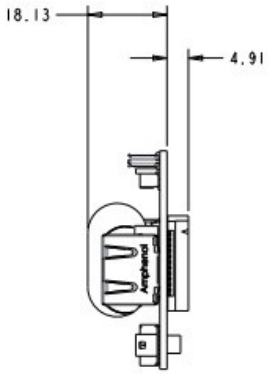


Drawings—Preliminary

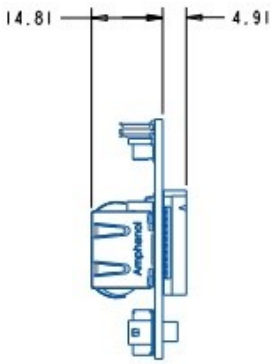


121.6 mm

0.00



Edgeview with large RTC battery backup



Edgeview with small or no RTC battery backup

Standard Pinout

J1				J2			
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	Vs1	2	Vs2	1	Analogue1	2	Analogue2
3	Vs3	4	12V_AUX	3	SDA2	4	TEMP1
5	-12V_AUX	6	SYSRESET#	5	SCL2	6	TEMP2
7	NVMRO	8	SYSRESET	7	TEMP4	8	TEMP3
9	NVMRO# / CMM_RESETI_n	10	MASKRESET#	9	MP16_TXD [40]	10	MP14_TXD [36]
11	GDISCRETE1	12	MASKRESET	11	MP16_RXD [39]	12	MP14_RXD [35]
13	GDISCRETE1# / CMM_RESETO_n	14	VBAT	13	MP10_TXD [28]	14	MP15_TXD [38]
15	GA0#	16	GA1#	15	MP10_RXD[27]	16	MP15_RXD [37]
17	GAP#	18	SM2	17	MP11_TXD [30]	18	MP11_RXD [29]
19	SM0	20	SM3	19	MP9_TXD [26]	20	MP8_TXD [24]
21	SM1	22	GPIO4	21	MP9_RXD [25]	22	MP8_RXD [23]
23	GPIO1	24	GPIO5	23	MP12_TXD [32]	24	MP12_RXD [31]
25	GPIO2	26	GPIO6	25	MP7_TXD[22]	26	MP6_TXD [18]
27	GPIO3	28	SDA3	27	MP7_RXD [21]	28	MP6_RXD [17]
29	MRI_RXD	30	SCL3	29	MP13_TXD [34]	30	MP13_RXD [33]
31	MRI_TXD	32	GND	31	MP5_TXD [16]	32	MP4_TXD [14]
33	GND	34	3.3V_AUX	33	MP5_RXD [15]	34	MP4_RXD [13]
35	1000BaseT.DA.P	36	1000BaseT.DB.P	35	GPIO19 [TACH3]	36	GPIO20 [PWM3]
37	1000BaseT.DA.N	38	1000BaseT.DB.N	37	MP3_TXD [12]	38	REDUN_CIN
39	GND	40	3.3V_AUX	39	MP3_RXD [11]	40	REDUN_COUT
41	1000BaseT.DC.P	42	1000BaseT.DD.P	41	CHM_CONSOLE_TXD	42	PSU_INHIBIT1
43	1000BaseT.DC.N	44	1000BaseT.DD.N	43	CHM_CONSOLE_RXD	44	PSU_ENABLE1
45	GND	46	3.3V_AUX	45	GA2	46	PSU_FAIL1
47	1000BaseKX.RX.P	48	1000BaseKX.TX.P	47	PSU_INHIBIT3	48	PSU_INHIBIT2
49	1000BaseKX.RX.N	50	1000BaseKX.TX.N	49	PSU_ENABLE3	50	PSU_ENABLE2
51	GND	52	3.3V_AUX	51	PSU_FAIL3	52	PSU_FAIL2
53	MP1_TXD [8]	54	MP1_RXD [7]	53	ISOL_PWR	54	ISOL_GND
55	GND	56	3.3V_AUX	55	PWM1	56	PWM2
57	MP2_TXD [10]	58	MP2_RXD [9]	57	FAN_RTN	58	FAN_PWR
59	GND	60	3.3V_AUX	59	TACH2	60	TACH1

General Information

FPGA and Main Memory

PolarFire FPGA from Microchip, MPFS095T

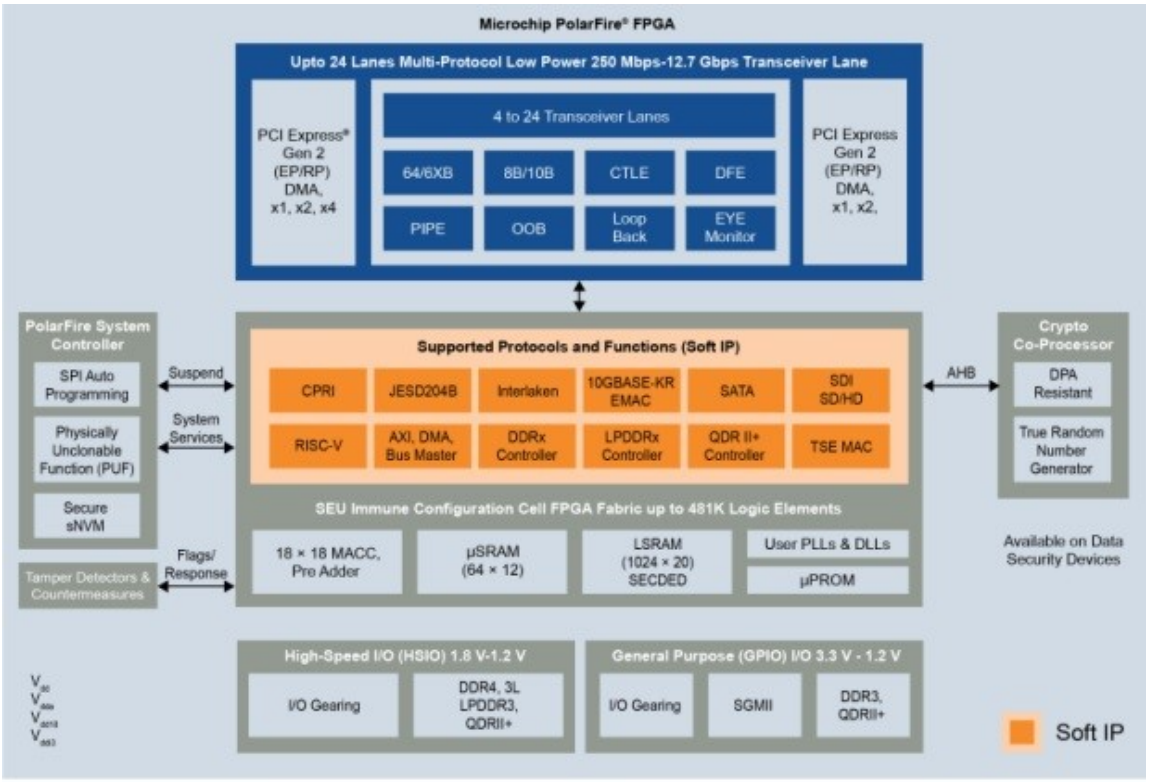
• 4 GB SDRAM
• 64 GB EMMC

General Information

• Highly configurable design
• Supports up to 16 backplane slots
• Up to 16 MP ports (can also be used for GPIO)
• Up to 40 GPIO available
• Up to 4 direct analog temperature sensor interfaces (options for more available) and up to 2x I2C ports
• 3x remote LEDs that are configurable (can support Over-temp, Fan Fail, and Power Status for example)
• Supports RESTful Web Service and Remote Management Control Protocol (RMCP) . REST resources include text, JSON, XML
• Supports GDISCRETE, NVMRO, and SYSRESET outputs

External Interfaces

• Supports up to 16 backplane slots
• Directly supports up to 3 Fan interfaces (PWM, etc) and up to 3 Power Supply Units (PSUs)
• External interfaces include 3 LEDs, 1x USB port, 1x Ethernet 10/100/1000BASE-T port. 1000BASE-KX is also accessible via the backplane only



Technical data in this datasheet is subject to change. Consult factory for details.

System Management Interface

The Ethernet (10/100/1000 Base-T and KX) interface supports Remote Management Control Protocol (RMCP) sessions based on IPMI v1.5 that allow System Management Software (like IPMItool and higher-level software using OpenIPMI) to interact with the Chassis Manager and underlying FRUs using standard IPMI and VITA 46.11 messages.

Chassis Control

Chassis Manager Hard Reset (Reboot)
IPMI/CLI command or user defined input (ChMC GPIO)

Chassis Activation

IPMI/CLI command or user defined input (ChMC GPIO)
Scripting for power-up and shut-down sequences
Orderly Power-up
Orderly Shut-down
Power-Cycle

Optional – control for INHIBIT* signal

Kill command (immediate shut-down)
Optional – monitor input power available
Optional – payload power good (discrete or 'sensor based')
Optional – safety interlock input o Chassis Hard Reset
IPMI/CLI command or user defined input (ChMC GPIO)
Initiate FRU CONTROL[Cold Reset] request to each FRU
Optional – pulse SYSRESET* signal

Chassis Diagnostic

IPMI/CLI command or user defined input (ChMC GPIO)
Initiate FRU_CONTROL[Diagnostic IRQ] request to each FRU
Optional – pulse user defined signal (ChMC GPIO)

Chassis LED support

Up to 3 VITA 46.11 LEDs with 1-wire or 2-wire connections (3 color)
ChM State, Payload Power State, Health State, User Defined - Event Handling - Enable/Disable ChM's System

Event Logging

Choose: none, all, critical, selected sources: sensor_types
Enable/Disable event forwarding (push) to SMI

Select number of SEL entries to store

Linear – overflow or keep N when full (volatile)
Circular – over-write oldest when full (volatile)
Cache – Non-volatile, save N entries/file

Updates VITA 46.11 sensors for each FRU based on events (and periodic polling)

 ChM implements VITA 46.11 sensors that 'aggregate' readings across all FRUs Updates Cooling Management settings based on Temperature events o Enable/Disable Platform Event Filtering (PEF) Take Chassis Control actions OEM actions Send FRU_CONTROL[x] command Pulse user defined GPIO[x] External Alerts are not currently supported

Icicle Development Kit

Configured with software for SHM300
Comes with cabling to a OpenVPX backplane header
SHM300-30-XXX (see ordering options on configuration page)

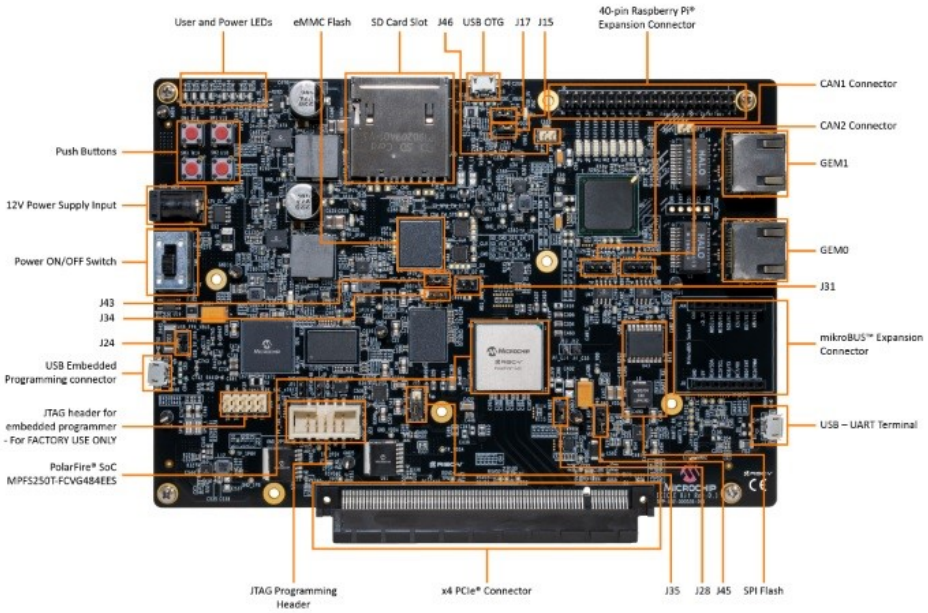
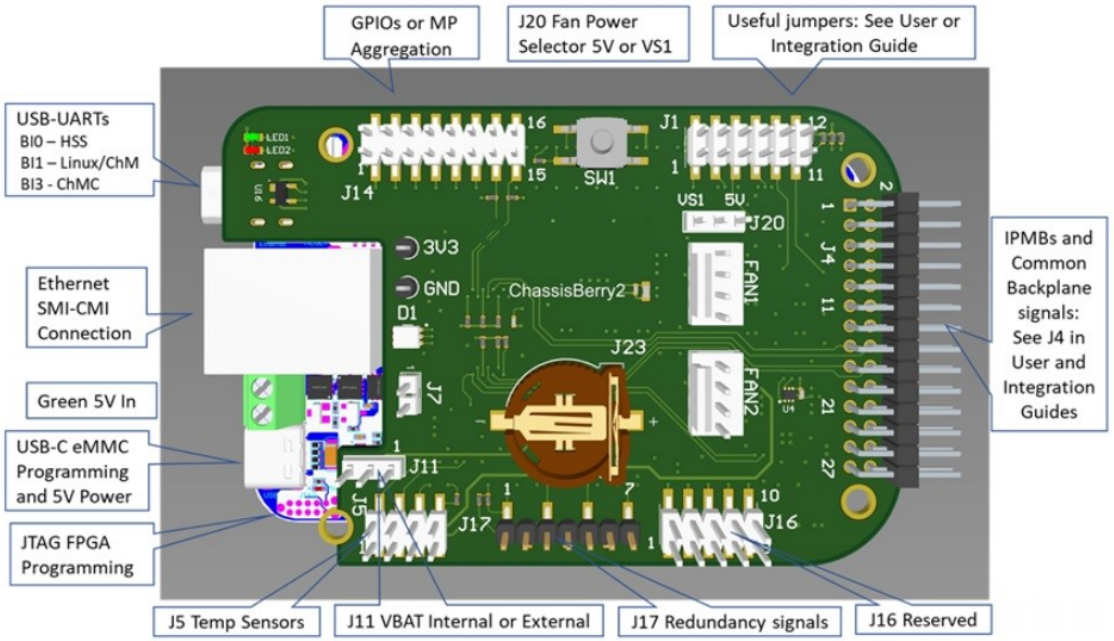


Image courtesy of Microsemi

ChassisBerry2 Development Kit (Diagram Below is Preliminary)

Configured with software for SHM300
Comes installed in a Pixus chassis and cabled the OpenVPX backplane
SHM300-40-XXX (see ordering options on configuration page)



Ordering Options
SHM300 Hardware Management Card

SHM300-A0-CDE-XX

A = ShMM Controller

0 = SHM300 Mezzanine, affixes to rear of backplane
1 = ChassisBerry dev kit (EOL lab/test version, no longer available for new designs)
2 = Pluggable version, consumes a VPX slot
3 = Icicle Polarfire SoC dev kit, desktop lab/test version, cables to backplane
4 = ChassisBerry2 dev kit, lab/test version (installable in most lab chassis)

2 digit customization code

Blank = standard, no customization

C = Real Time Clock (RTC) Battery Backup

0 = None
1 = 1 Farad
2 = 5 Farad
3 = Other

D = Temperature Range

0 = Commercial (0 C to +70 C)
1 = Industrial/MIL (-40 C to +85 C)
2 = Other

E = Conformal Coating

0 = None
1 = Humiseal 1A33 Polyurethane
2 = Humiseal 1B31 Acrylic